REMARKS

Summary Of The Office Action & Formalities

Claims 1-5 are all the claims pending in the application. By this Amendment, Applicants are amending claims 1 and 3 to correct minor typographical errors to the parenthetical reference numerals.[1]

Applicant thanks the Examiner for initialing the references listed on form PTO-1449 submitted with the Information Disclosure Statement filed on January 6, 2000.

The Examiner has acknowledged Applicant's claim to foreign priority, but has indicated that the USPTO has not received a copy of the priority document. **The Examiner is kindly requested to recheck Applicant's file and consult with the PCT branch at the USPTO to confirm that the International Bureau has sent (and the USPTO has received) a copy of the certified copy of the priority document.**

The drawings are objected to for the reasons set forth at page 2 of the Office Action. Applicant is submitting herewith proposed drawing changes to Figs. 1 and 4A, labeling these figures as "Prior Art." Applicant is also amending the Specification to clarify the description of Figs. 4A and 4B.

With respect to Fig. 4B, Applicant disagrees that this figure discloses only that which was in the prior art. To the contrary, Fig. 4B is not prior art, since the switching architecture is different from the Clos network illustrated in Fig. 1. In particular, Fig. 4B is a specific example

[1] Applicant understands that the USPTO may, on its own, delete the parenthetical reference numerals in the claims prior to issuing a patent.

of the network of Fig. 3 and, therefore, must be viewed in the context of Fig. 3. Indeed, the number of inputs and outputs for each matrix and the associated exclusive relationship between the inputs and outputs of each first and last stage matrix as explained at page 9 of the specification are specific examples of the generalized network of Fig. 3 and are different from that of a Clos network. These differences, alone, are sufficient to prevent the figures from being characterized as disclosing prior art.

Applicant is also amending the specification to correct minor typographical errors.

The prior art rejections are summarized as follows:

1. Claims 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's cited document by Wong et al.

2. Claims 2-3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong in view of Petersen (USP 5,467,347).

Applicant respectfully traverses.

Claim Rejections - 35 U.S.C. § 102

1. Claims 1 And 4 In View Of Wong et al.

In rejecting claims 1 and 4 in view of Wong et al., the grounds of rejection state that

> Regarding claim 1, Wong teaches devices for switching ATM cells (figures 1-3 - reference herein will be made specifically to figure 1) establishing a single path per virtual circuit having N.R inputs (k.n inputs) and N.R outputs (l.p outputs), N and R (k or l and n or p) being two integers not less than two, the device comprising at least two stages, including an inlet stage (n x m stage) having R.N sets (n.k sets) of Q outputs (r) and an outlet stage (s x p stage) having R.N sets (p.l sets) of Q' inputs (r) -- wherein n=p, m=n, and m=s (see page 709, col. 1, lines 4 and 17) and along the same logic k=l, thus n=m=s=p=R and k=l=N.

Furthermore, the above is characterized in that for the flow of data carried by any intermediate link (r) that is part of the single path set up between an input and an output to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input of the inlet stage (n x m stage) can be connected to an output of the inlet stage which can be selected only from Q outputs (r) exclusively associated with that input; and in that each output of the outlet stage (s x p stage) can be connected to an input of the outlet stage which can be selected only from Q' inputs (r) of the output stage exclusively associated with that output.

Regarding claim 4, Wong teaches a switching device (figure 3) according to claim 1 including an inlet stage (n x m stage), a central stage (1 x 1' stage), and an outlet stage (m' x n' stage) characterized in that Q and Q' (r and r') are equal to R (see page 709, col. 2, line 17 and page 710, col. 1, line 10 wherein l=l' and m=m' and therefore r=r'=(Q=Q')=m=R), the central stage (1 x 1' stage) includes R^2 matrices (r=r', therefore the l x l' stage includes r^2 or R^2 matrices), and the matrices of the inlet stage and the matrices of the central stage are organized into R sets (k sets, where k may be equal to r) each including N matrices (h matrices) of the inlet stage and R matrices (g matrices, where g may be equal to m) of the central stage and the matrices of the outlet stage are organized into N sets (h' sets) of R matrices (m' matrices, where m' may equal r').

Furthermore, the above is characterized in that each of the R.N matrices of the inlet stage (n x m stage) has a single input (i.e., let n=1) and R outputs (m outputs), each of the R^2 matrices of the central stage has N inputs and N outputs (l inputs and l' outputs) -- the inputs being respectively connected to an output of each of the matrices of the inlet stage that belong to the same set of matrices, and each of the R.N matrices of the outlet stage (m' x n' stage) has R inputs (r' inputs) and a single output (i.e., let n'=1), those R inputs (r' inputs) being connected to outputs respectively belonging to the R sets of matrices of the central stage and of the inlet stage.

Office Action at pages 3-4. Applicant respectfully disagrees.

As a preliminary matter, contrary to the Examiner's position, Fig. 1 and the related text of Wong do not teach setting the value of m equal to n for the m x n matrix. The Examiner references page 709 for this disclosure, however, the discussion at page 709, second paragraph, in which it is disclosed that m = n in one example, is, with respect to the three stage network architecture of Fig. 2, not the two-stage network architecture of Fig. 1. In fact, at column 2 of page 708, Wong teaches that it is preferred to have the ratio e = m/n to be greater than 1. This would clearly teach away from having m = n.

More significant is the lack of any disclosure in Wong of the requirement in claim 1 that "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input; and in that each output . . . of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs . . . of the outlet stage exclusively associated with that output." This feature is illustrated, for example, in Fig. 3 of the present application. Input link 312_1, for example, is exclusively associated with output links $313_{1,1}$ to $313_{1,R}$, and is not associated with output links $313_{R,1}$ to $313_{R,R}$.

As explained at page 1, lines 28-30 of Applicant's specification, in a Clos network, each of the intermediate stage matrices is connected to one of the outputs of each of the inlet stage matrices. That is, in a three-stage Clos network, every first or inlet stage switching module has one and only one connection to each of the second stage modules. This is also true for the third stage switching module. Moreover, each of the input links for each inlet matrix can be

associated with any of the output links of that matrix. Similarly, each of the output links for each last stage matrix can be associated with any of the input links of that matrix.

Regarding claim 4, the Examiner's rejection is based on the assumption that "each of the R.N matrices of the outlet stage (m' x n' stage) has R inputs (r' inputs) and a single output (**i.e., let n'=1**) . . . ." (Emphasis added). The Examiner has not pointed to any disclosure that would teach or suggest using inlet matrices, each having a 1 x m matrix architecture, and outlet matrices, each having an m x 1 matrix architecture. Wong simply lacks sufficient specificity to constitute anticipation of claim 4. See Manual Of Patent Examining Procedure ("MPEP") at Section 2131.03. Indeed, one skilled in the art would not have envisaged the particular architecture required by claim 4 based on the generalized disclosure of Wong. To the contrary, one skilled in the art would understand the disclosure of Wong as requiring n to be set to a number greater than 1, since this would have been the conventional architecture for the disclosed networks in Wong.

In view of at least the foregoing distinctions, claims 1 and 4 are believed to be allowable over the prior art, and the Examiner is kindly requested to reconsider and withdraw the rejection of these claims.

Claim Rejections - 35 U.S.C. § 103

1. Claims 2-3 And 5 In View Of Wong And Petersen.

In rejecting claims 2, 3 and 5, the Examiner acknowledges that Wong fails to disclose the additional features recited in these claims, but argues that such features would have been obvious in view of Petersen. Applicant respectfully disagrees.

First, claims 2, 3 and 5 are believed to be allowable at least by reason of their respective dependencies.

Second, Applicant submits that the Examiner has not set forth sufficient grounds to establish the requisite motivation to combine the two references in the manner alleged to satisfy the rigorous standard set forth in In re Sang Su Lee, 2002 U.S. App. LEXIS 855.

That is, the current grounds of rejection do not present the required showing that the claimed invention would have been obvious in view of the combination of Wong and Peterson. At best, Wong and Peterson each disclose separate comprehensive network architectures.

That is, one skilled in the art would understand the disclosure in Wong to teach a complete and integrated system. The same with the disclosure in Peterson. There simply is no disclosed teaching for selectively picking and choosing certain features from the integrated system of one reference and combining them with those of the other, and no guidance from the art on which specific features should be selected and which should be discarded.

Moreover, the Examiner has not set forth a technically cogent formulation for applying the architecture of Peterson to that of Wong in order to achieve the invention as recited in claims 2, 3 and 5.

For example, with respect to claim 2, the Examiner characterizes the switchcore 12 as the recited outlet stage. However, in Peterson, switchport 11B is the output side that receives data from the switchcore 12.

Regarding claim 3, a simple comparison of the recited network architecture as graphically illustrated in Applicant's Fig. 3 with the disclosures of Wong and Peterson, clearly

demonstrates that one skilled in the art would not have arrived at the claimed invention based on these two references.

Instead, the grounds of rejection make multiple assumptions and technically mischaracterize the applied references to argue that the claimed invention is obvious. Indeed, the grounds of rejection can point to no more than the generalized overlap in the field of endeavor as motivation for making the selective, specific, proposed modification. Absent hindsight, however, this generalized overlap gives no guidance whatsoever in picking and choosing the selective, specific features for modification.

"The test for combining references is what the combination of references taken as a whole would suggest to one of ordinary skill in the art." In re Simon 174 USPQ 114 (CCPA 1972. However, rather than properly considering the teachings of the references as a whole, the grounds of rejection selectively pick and combine features from the applied references in a fashion that is certainly not taught or suggested by the references, whether taken individually or in combination. It is only after having the benefit of Applicants' own disclosure that one could try to selectively lift certain features from the two applied references to piece together Applicants' invention recited in claims 2, 3 and 5, since neither applied reference, nor any other teaching of record, provides the requisite motivation for such selectivity. However, even when armed with this improper hindsight, one must further characterize the disclosure in a way that is technically incorrect in order to try and argue Applicant's claimed combinations.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Submitted herewith is a Petition For Extension Of Time with fee and an Excess Claim Fee Payment Letter with fee.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 6, paragraph beginning at line 34 is amended as follows:

Figures 4A and 4B show an advantageous structure based on the network from Figure 3 [allowing broadband transfers (Figure 4B) and narrowband transfers (Figure 4A); and], with Fig. 4A showing a known device allowing narrowband transfers, and Figure 4B showing a device according to the invention and which allows wide band transfers, this latter device being able to be derived from incomplete prior art matrices and by restricting routing in these derived prior art matrices to allow broadband transfers (Figure 4B) and narrowband transfers (Figure 4A); and

Page 7, paragraph beginning at line 21 is amended as follows:

The input matrices [21_i] 211_i are organized so that the incoming flux of data at each input 212_i can be directed to any matrix [22_i] 221_i of the outlet stage. In other words, a tree structure is used which can define N possible connections for each input and not more than N (N is the number of matrices in the outlet stage in this embodiment).

Page 8, paragraph beginning at line 20 is amended as follows:

The links between the various stages are organized so that the flow received by each input of a matrix 311_i of the inlet stage can be transmitted to any of the corresponding R matrices $321_{i,1}$ through $321_{i,R}$. Similarly, each output of a matrix [311_i] 331_i can receive data from each matrix 321_k of the central stage. To be more precise, each output link [333_{ii}] 333_i can receive data from any of the R matrices $321_{1,i}$ through $321_{R,i}$.

IN THE CLAIMS:

The claims are changed as follows:

Claim 1. (Amended) A device for switching ATM cells establishing a single path per virtual circuit, having N.R inputs and N.R outputs, N and R being two integers not less than two, the device comprising at least two stages, including an inlet stage (21; 31; 411_1, ..., 411_R) having R.N sets of Q outputs (213_{11}; 313_{11}; 413_{11}) and an outlet stage [(22; 33; 421_1, ..., 422_R, ...)] $(22; 33; 421_1, \ldots, 422_1, \ldots)$ having R.N sets of Q' inputs [(223_1; 333_i; 442_1)] $(222_1; 332_{1,1}; 423_{1,1})$,

characterized in that for the flow of data carried by any intermediate link (213_i, 222_j; 313_i, 332_j, 413_i, 423_j) that is part of the single path set up between an input and an output to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input (212_1; 312_1; 412_1) of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs (213_{11}, ..., 213_{R1}; 313_1, ..., 313_{1R}; 413_{11}, ..., 413_{1R}) exclusively associated with that input; and

in that each output [(223_1; 331_i; 422_1)] $(223_1; 333_i; 442_1)$of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs (222_{11}, ...,

222_{1R}; 332_{11}, ..., 332_R1_1; 423_{11}, ..., 423_{1R}) of the outlet stage exclusively associated with that output.

Claim 3. (Amended) A switching device according to claim 1 including an inlet stage (31), a central stage (32), and an outlet stage (3); characterized:

- in that, Q being equal to R, the inlet stage (31) comprises N matrices (311_l, ...) each having R inputs (312_l, ...) and R^2 outputs (313_{11}, ...), those outputs being organized into R sets of R outputs each corresponding to one of said R inputs, and in that each input (312_l) of that matrix can be connected to an output of that matrix which can be selected only from R outputs (313_{ll}, ..., 313_{Rl}) of the set of outputs corresponding to that input;

- in that the central stage (32) comprises R sets of R matrices (321_{11}, ...) each having N inputs and N outputs, the R outputs of each set of outputs of the inlet stage being connected to inputs belonging to the same set of R matrices of the central stage; and

- in that, Q' being equal to R, said outlet stage (33) comprises N matrices (331_l, ...) each of those matrices having R^2 inputs (332_l, ...) and R outputs (333_l, ...), those R^2 inputs being organized into R sets of R inputs, each set respectively corresponding to one of those R outputs; and in that each output [(323_l, ...)] <u>(333_l, ...)</u> of that matrix can be connected to an input of that matrix which can be selected only from R inputs [(322_{ll}, ..., 322_{Rl})] <u>(332_{ll}, ..., 332_{Rl})</u> of the set of inputs corresponding to that output; and in that the R inputs (322_{ll}, ..., 322_{Rl}) of each set are respectively connected to R outputs respectively belonging to the R sets of matrices of the central stage (32).

PRIOR ART

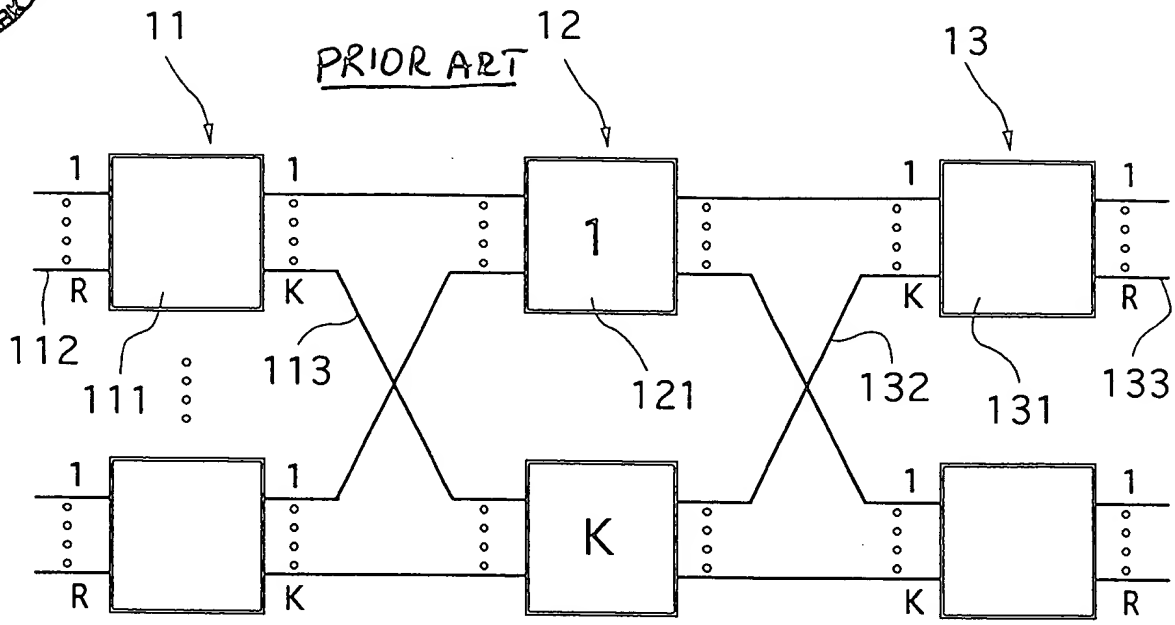


Fig. 1

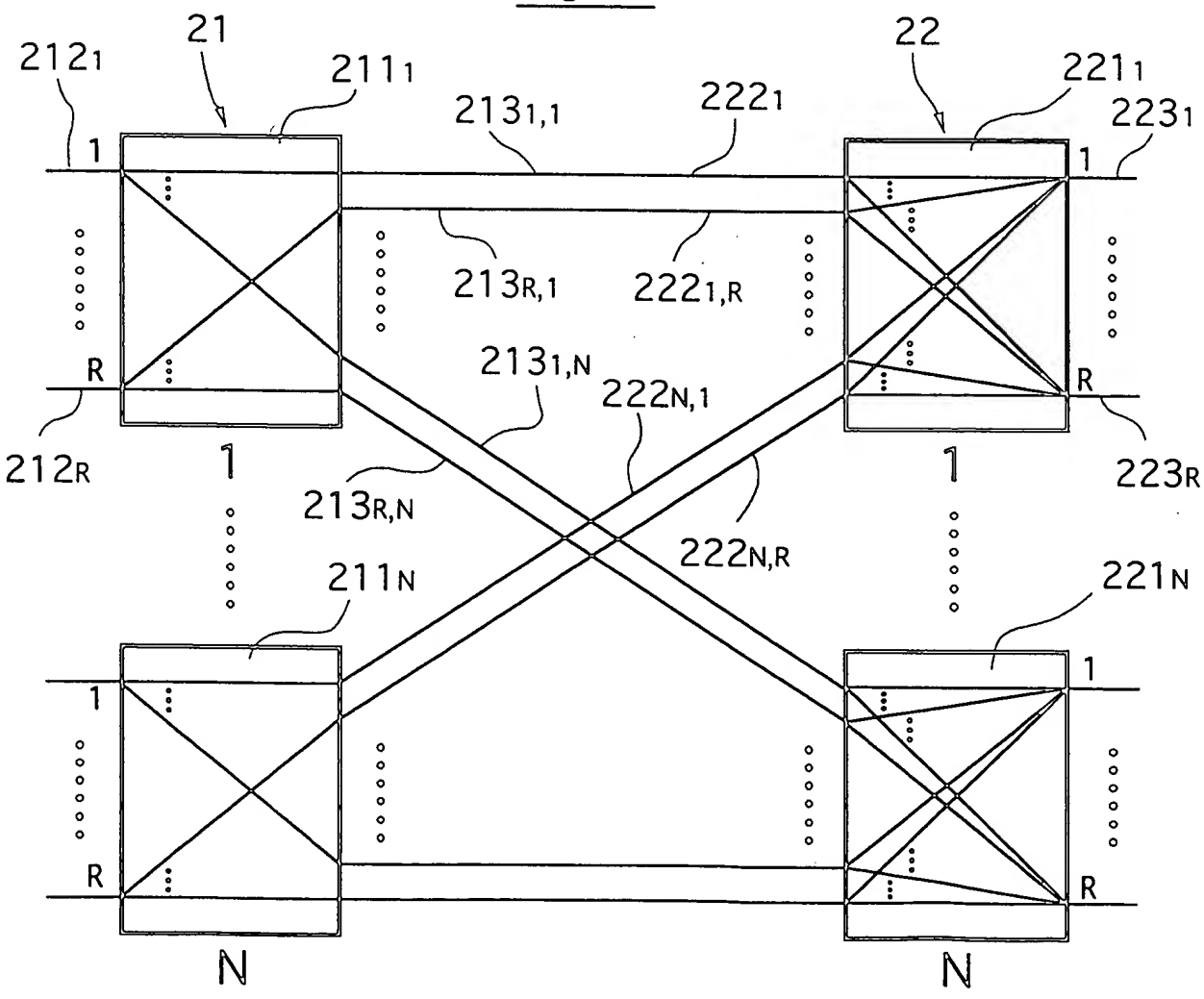
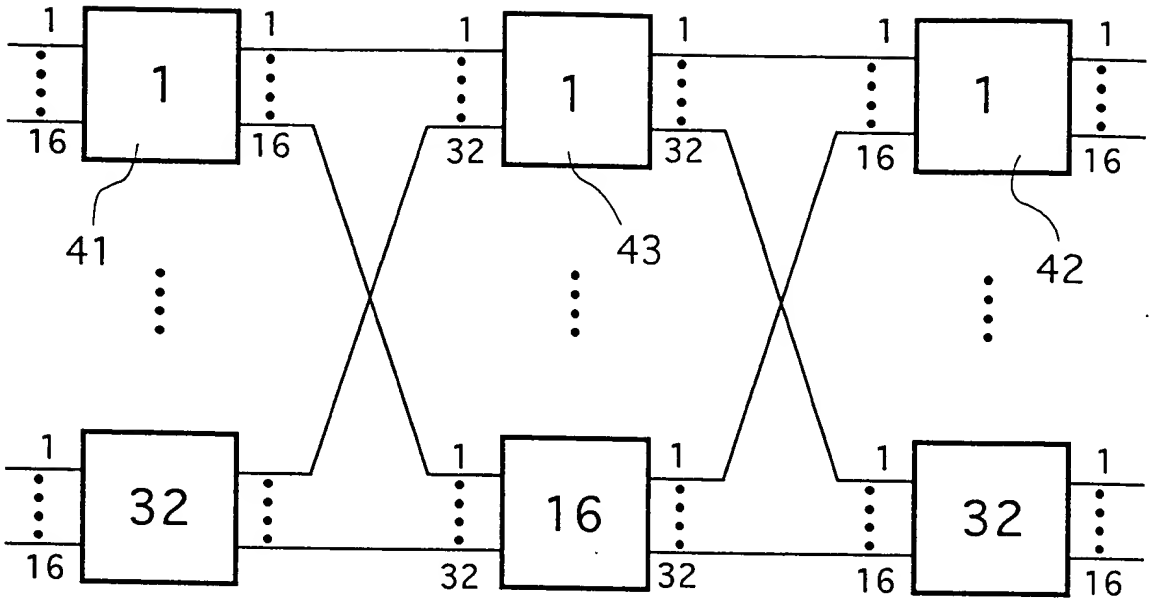


Fig. 2



PRIOR ART

Fig. 4A

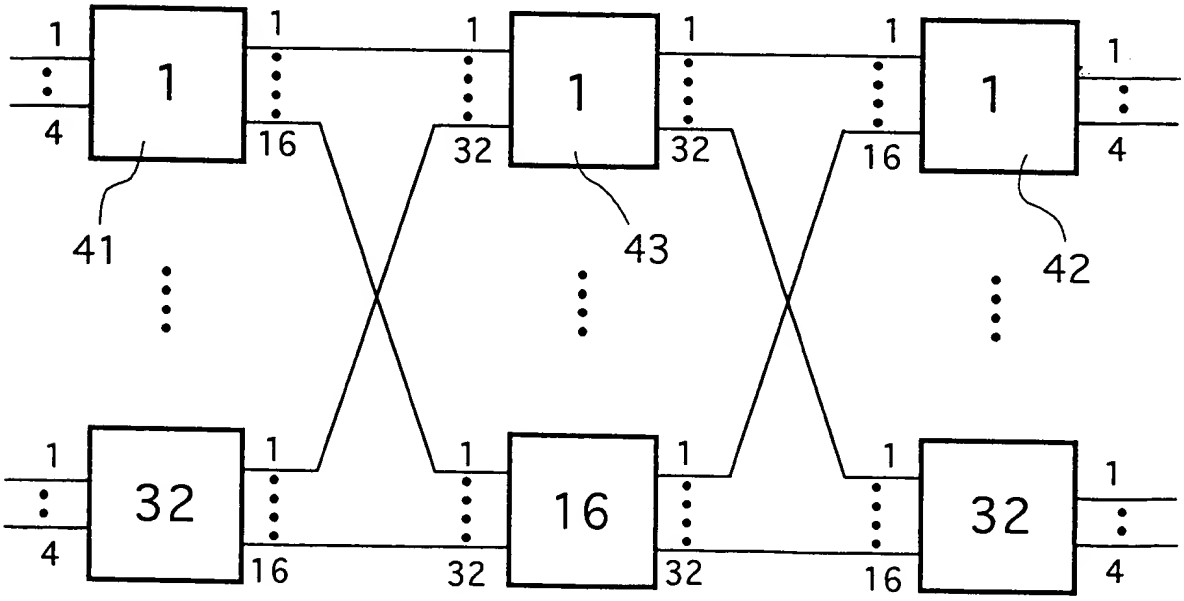


Fig. 4B